A Flexible Model of a CMOS Field Programmable Transistor Array Targeted for Hardware Evolution

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Abstract*. This article focuses on the properties of a fine grained re-configurable transistor array currently under test at the Jet Propulsion Laboratory (JPL). This Field Programmable Transistor Array (FPTA) is integrated on a Complementary Metal-Oxide Semiconductor (CMOS) chip. The FPTA has advantageous features for hardware evolutionary experiments when compared to programmable circuits with a coarse level of granularity. Although this programmable chip is configured at a transistor level, its architecture is flexible enough to implement standard analog and digital circuits' building blocks with a higher level of complexity. This model and a first set of evolutionary experiments have been recently introduced. Here, the objective is to further illustrate its flexibility and versatility for the implementation of a variety of circuits in comparison with other models of re-configurable circuits. New evolutionary experiments are also presented, serving as a basis for the authors to devise an improved model for the FPTA, to be fabricated in the near future.*

1 Introduction

In the context of Evolvable Hardware (EHW), researchers have been using programmable circuits as platforms for their experiments. These programmable circuits are divided into two classes, Field Programmable Gate Arrays (FPGAs) and Field Programmable Analog Arrays (FPAAs). The former is intended to be used in the digital domain, and the latter in the analog domain. Both the *FPGAs* and the *FPAAs* commercially available have a coarse granularity, which may restrict the potential of evolutionary design to the achievement of well-known topologies that are possible with such components. In order to overcome this problem, a fine-grained model of a programmable circuit is being tested at JPL. This programmable device, called the FPTA, provides the benefits of reconfiguration at the transistor level, the use of CMOS technology, and the possibility of synthesizing circuits in the analog

and in the digital domain. A first version of this programmable chip has already been successfully employed in the evolution of a computational circuit [11].

The purpose of this paper is twofold: to highlight the advantages of a fine-grained reconfigurable architecture that is also able to provide circuits with higher levels of granularity as building blocks for evolution; and to present preliminary evolutionary experiments involving the synthesis of circuits whose main characteristics are analyzed in different domains. The capacity of mapping circuits of higher complexity, while still being programmable at the transistor level, gives the designer the possibility to choose the most adequate building blocks to be manipulated by the evolutionary algorithm. Additionally, the evolution of circuits in different analysis' domains shows the flexibility of this model to accomplish the synthesis of a wide variety of electronic circuits.

This paper is divided in the following way: section 2 briefly summarizes some models of programmable circuits; section 3 reviews the basic features of the programmable device developed at JPL; section 4 describes the mapping of some standard circuit building blocks into this FPTA; section 5 presents two evolutionary experiments, where the FPTA is used as a model to synthesize circuits in different domains of analysis. An enhanced model of the FPTA is also introduced in this section. Section 6 concludes the work, and describes future developments and applications of this reconfigurable platform.

2 Reconfigurable Circuits

Field Programmable Analog Arrays and *Field Programmable Gate Arrays* promise to establish a new trend in electronic design, where a single device now has the flexibility to implement a wide range of electronic circuits. While FPGAs have been developed for applications in the domain of digital signal processing and re-configurable computing, most FPAA models are being developed for applications in programmable mixed-signal circuits and filtering. In addition to the intrinsic flexibility of these devices, which confers advantageous features to standard electronic design, FPGAs and FPAAs are also the focus of research in the area of *self programmable* systems [3][7][12]. Particularly, genetic algorithms are the main agents employed to promote the property of automatic configuration.

Nevertheless, there are many issues that should be addressed prior to using a programmable circuit in the context of artificial evolution. Perhaps, the most important of these issues is that of granularity of the programmable chip. The devices presented so far can be divided into two classes, coarse grained and fine grained. While the former uses more complex circuits, such as digital gates and operational amplifiers, as the building blocks for the design process, the latter is configurable at a lower level, usually at the transistor level.

Most FPGA models consist of an arrangement of cells that perform digital logic, such as basic gates, multiplexers and flip-flops [7]. The user can configure the cells' connections and, in some models, their functionality. Many surveys of FPGA models can be found in the literature [9]; therefore, this section focuses on the description of FPAAs, whose development has occurred more recently. Five models are described here.

2.1 TRAC – Totally Reconfigurable Analog Hardware

This device is a coarse grained FPAA, consisting of twenty operational amplifiers laid out as two parallel sets of ten inter-connectable amplifiers [2]. The Zetex programmable chip has been used in evolutionary experiments that targeted the synthesis of computational functions [2], rectifiers, and others [8]. The main limitation of the use of this chip in EHW is that evolution is constrained to the arrangement of high level conventional building blocks to compose the final topology, not being able to arrive at any novel design.

2.2 Motorola Field Programmable Analog Array (MPAA020)

The analog resources of the coarse grained MPAA020 [4] are distributed along 20 nearly identical cells. Each cell includes the following hardware resources: one CMOS operational amplifier; one comparator; capacitors; programmable switches; and SRAM. This is the hardware required for the design of switched capacitor based circuits. This FPAA is configured by a bitstring of 6864 bits that control the circuit connectivity, capacitors' values and other features. This programmable chip has been used as a platform for the evolution of filters, oscillators, amplifiers, and rectifiers [13]. The MPAA020 provides more resources for evolution, since programmable capacitors and resistors (implemented through the switched capacitor effect) are now included on chip. However, since the basic building blocks are fixed to Operational Amplifiers (OpAmp) topologies, there is little room for evolution to arrive at novel designs. Another limitation of the current version of this chip is that it is not a transparent architecture, preventing simulation/analysis of evolved circuits.

2.3 Palmo (University of Edinburgh)

The Palmo development system [1] is BiCMOS technology coarse-grained FPAA chip that works on pulse-based techniques. The chip architecture consists of an array of programmable cells that perform the functionality of integrators. One of the design goals is to use the chip in EHW experiments, employing GAs to determine the integrators' interconnectivities and their gains.

2.4 Evolvable Motherboard (University of Sussex)

The Evolvable Motherboard (EM) [5] is a research tool designed for access at low level granularity. This programmable board allows different components to be plugged in as basic circuit elements. The board is organized as a matrix of components, where digitally controlled analog switches allow row/column interconnection. In total, approximately 1500 switches are used, giving a search space of 10^{420} possible circuits. The EM has already been used in evolutionary experiments whose objectives were the design of inverter gates, amplifiers and oscillators. In these experiments, bipolar transistors were the components manipulated by the evolutionary system.

2.5 – Lattice Programmable Analog Circuits (PACs)

The Lattice PAC is a coarse-grained programmable analog circuit that was commercially introduced recently [6], intended for applications in filtering, summing/differencing, gain/attenuation, and conversion. The PAC cell includes instrumentation amplifiers, an active resistance and a programmable capacitor. The

major limitation for the application of this chip to EHW is the fact that it is programmed through non-volatile memory cells with limited number of program/erase cycles , around 100,000, insufficient for evolutionary experiments.

The devices previously described have limitations from the point of view of their suitability in implementing *Evolution Oriented Reconfigurable Architectures* (EORA). In the case of the commercial devices (TRAC, MPAA020 and Lattice), the main problems are their coarse granularity and, in some cases, the non-transparent architecture. Coarse granularity constrains evolution to sample designs based on human conceived building blocks. The academic research tools, EM and Palmo, are a board level solution and a coarse grained design respectively. EM has inherent flexibility, since components are added by human plug-in, but will require a decision of what resources would finally go on a VLSI chip.

3 Field Programmable Transistor Array (FPTA)

This section reviews the architecture of the FPTA (more details can be found in [10]) This transistor array combines the features of fine granularity, being programmable at the transistor level, with the architectural versatility for the implementation of standard building blocks for analog and digital designs.

The Field Programmable Transistor Array is a fine-grained reconfigurable architecture targeted for Evolvable Hardware experiments. The basic components are MOS transistors, integrated on a chip using 0.5-micron CMOS technology [10]. As both analog and digital CMOS circuits ultimately rely on functions implemented with transistors, the FPTA appears as a versatile platform for the synthesis of both analog and digital (and mixed-signal) circuits. Moreover, as will be demonstrated in the next section, the FPTA architecture is also flexible enough to provide more complex building blocks to the evolutionary system.

The FPTA cell is an array of transistors interconnected by programmable switches. The status of the switches (ON or OFF) determines a circuit topology and, consequently, a specific response. Figure 1 illustrates an example of an FPTA cell consisting of 8 transistors and 24 programmable switches. This cell consists of PMOS and NMOS transistors, and switch based connections. As will be further described in this paper, this cell architecture allows the synthesis of both standard and novel topologies for some basic circuits. According to the outcome of the experiments being currently performed, a slightly different architecture may be proposed for the next version of the FPTA.

The programmable switches are implemented with transistors acting as transmission gates. The switches can either be programmed for the implementation of minimal and maximal resistance values, by applying 0V and 5V at the transistors' gates, or they can be programmed to implement intermediate resistance values, by applying values between 0V and 5V at the transistors' gates. Preliminary experiments suggest that the use of intermediate values for switching control generates a smoother fitness landscape [11].

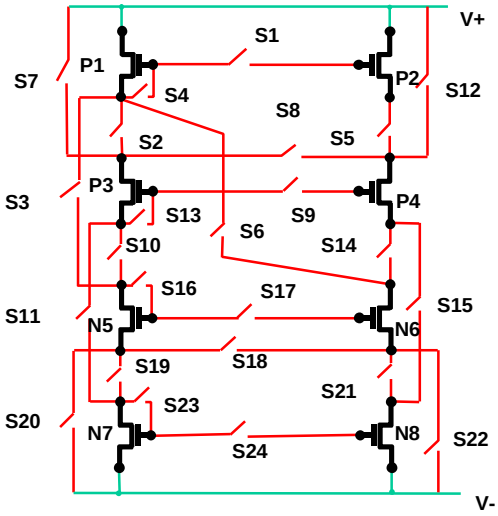

Fig. 1 – Schematic of a FPTA cell consisting of 8 transistors and 24 switches.

4 Mapping Standard Circuit Building Blocks Onto the FPTA

This section describes recent experiments performed with the FPTA chip, referring to the mapping of some standard circuit building blocks onto the FPTA. The objective is to show that the architecture depicted in Figure 1 is flexible enough to implement basic structures used in analog and digital design. We depict here the implementation of three cells: a basic common-source amplifier; a transconductance amplifier; and an AND digital gate. These are examples of circuits that can be optionally used as building blocks for the evolution of analog and digital circuits.

Figure 2.A depicts the FPTA configuration for a common source amplifier implementation. This circuit is employed to provide voltage gain. This structure can be easily mapped into one cell of the transistor array. As shown in the figure below, transistors P3 and P4 form a current mirror pair that works as the active load for the amplifying transistor, N6. The current level is determined by the input voltage *Vbias*, applied at the gate of the transistor N5, which serves as an active resistance for the current mirror. Figure 2.B compares the DC transfer function of these circuits in two cases: simulation and real implementation. In the former, we use PSPICE to simulate the amplifier without switches implementing the connections; in the latter, we get real data from the amplifier implementation.

From Figure 2 we can observe that the transfer curves of the two versions of the circuit have the shape of an inverter amplifier. They only differ in their higher saturation values, 5V for the simulated circuit and 4.6V for the real one. This difference is due to the fact that the circuit is very sensitive to the DC operating point, given by the bias current.

Another circuit building block that can be easily mapped into the FPTA is the transconductance amplifier, whose schematic is displayed in Figure 3. Also shown in Figure 3 is the graph comparing the DC transfer functions between the tranconductance amplifier implemented in the FPTA and a simulated version of the same with no switches.

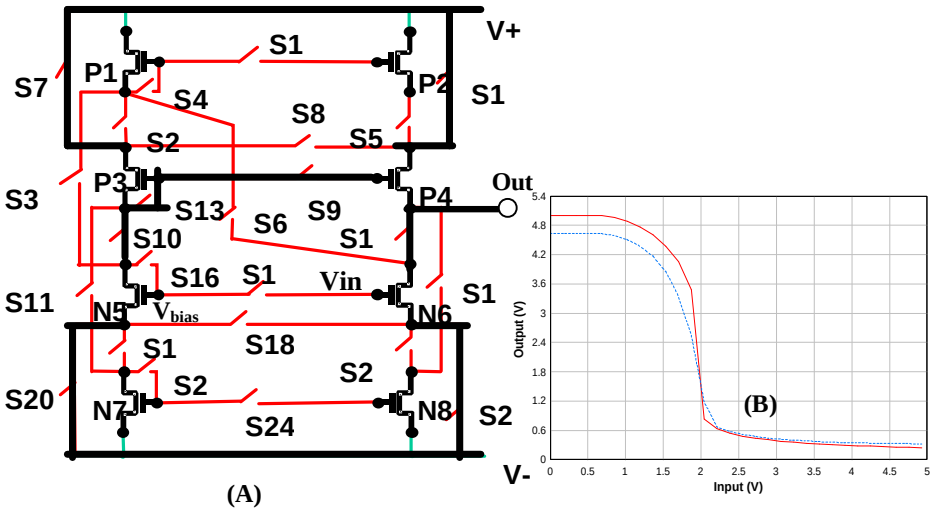

Fig. 2 – (A) - Schematic of the mapping of a basic common source amplifier onto the FPTA. (B) - DC transfer function of the common source amplifier in simulation (full line) and one implemented in the FPTA (dotted line).

Figure 4 displays the schematic of a digital gate mapped into two cells of the FPTA. This digital gate performs NAND/AND operations over the inputs *In1* and *In2*, as shown in the figure below. This circuit was implemented in the FPTA, and worked as expected.

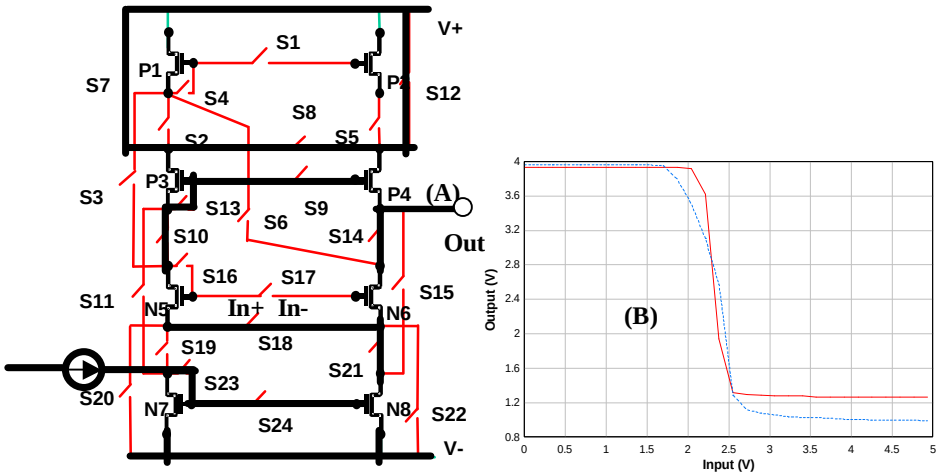

Fig. 3 – (A) - Schematic of a transconductance amplifier mapped onto the FPTA; (B) - DC transfer function of the circuit in simulation (full line) and implemented in the FPTA (dotted line).

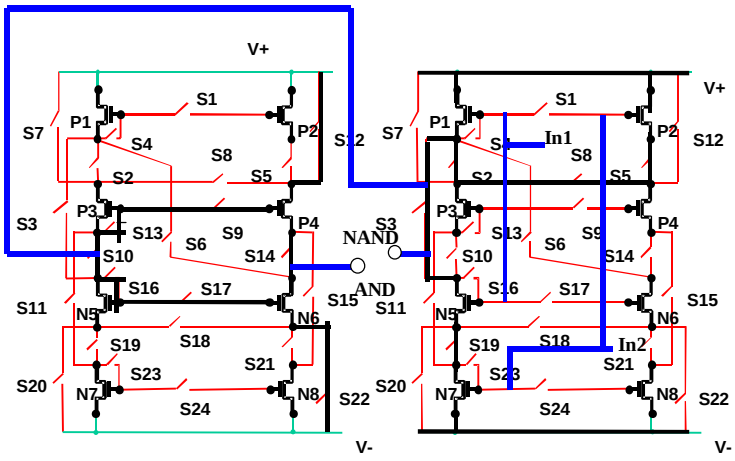

Fig. 4 – Schematic of an AND gate mapped into two FPTA cells.

5 Evolutionary Experiments

This section describes new evolutionary experiments carried out using the same FPTA model in the *PSPICE* simulator: the evolution of an amplifier and of a band-pass filter respectively. We employed a standard Genetic Algorithm with binary representation, 70% one-point crossover ratio and 4% mutation ratio.

In the first experiment, the objective was to synthesize a circuit with a DC transfer characteristic typical of an amplifier, similar to the ones illustrated in the last section.

The chromosomes were represented by 24 bit strings, where each bit maps the state (opened or closed) of one switch. The following fitness evaluation function was used:

$$\text{Fitness} = \text{Max}_{i=1}^{n-1} |V(i+1) - V(i)| \qquad (1)$$

Where V(i) describes the circuit output voltage as a function of the DC analysis index i, which spans the swept range of the input signal, i.e., from 0 to 5 Volts. This evaluation function aims to identify the maximum voltage gradients between consecutive input voltage steps, the larger the gradient, the larger the amplifier gain will be [12]. This fitness evaluation function does not impose a DC operating point for the amplifier. Figure 5 depicts the schematic of the evolved circuit, together with the DC transfer responses achieved in the FPTA implementation and in simulation.

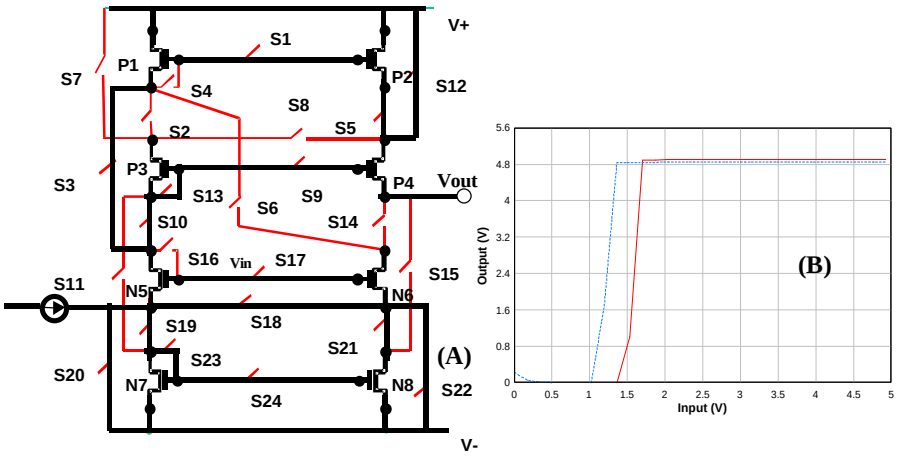

Fig. 5 – (A) - Schematic of an evolved amplifier using the FPTA model; (B) - comparison of the DC characteristic displayed by the simulated (full line) and implemented (dotted line) versions of the amplifier.

This result compares very well with the one reported in [12], where the same fitness function was used, but the basic elements for evolution were bipolar transistors and resistors. While around 10^4 evaluations were needed to obtain a similar DC transfer function in [12], only 900 evaluations (30 individuals along 30 generations in only one GA execution) were necessary using the FPTA. In addition, the evolved circuit shown above can be directly implemented in a CMOS reconfigurable chip.

The second evolutionary experiment targeted the synthesis of a band-pass filter for an AM band, with a range that goes from 150kHz to 1MHz. This experiment served as a testbed for an improved cell model for the FPTA. Since the basic FPTA cell does not include large capacitances (only low-valued parasitic capacitances), we included external capacitances in the original cell, based on a previously evolved filter [14]. This new model also included additional switches, which propagated the input signal to other points in the FPTA. Instead of using values of 0V and 5V to control the switches, intermediate values of 1.5V and 3.5V were employed in this experiment. It

has been verified that all of the above mentioned new features improved the performance of the FPTA for filter design. Figure 6 depicts the evolved filter and its frequency response.

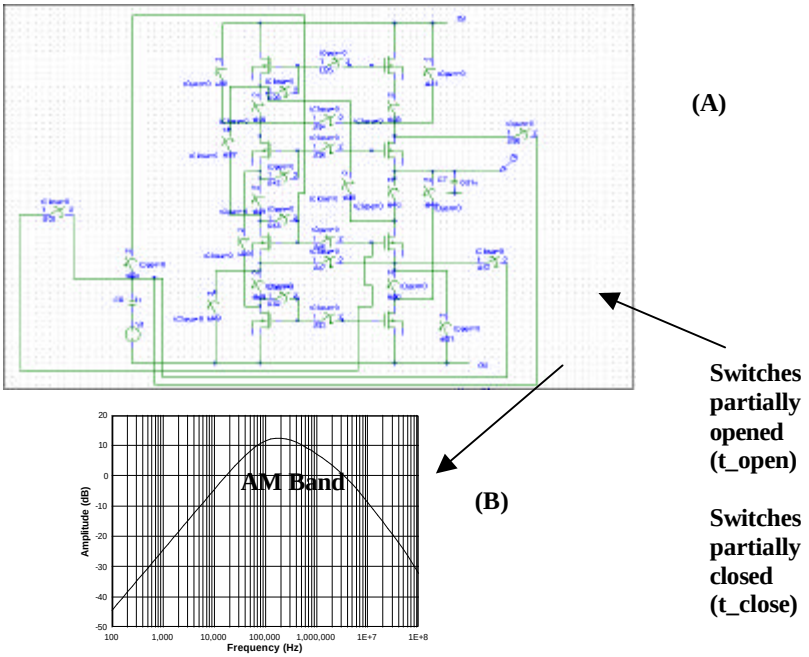

Fig. 6 – (A) - Schematic of an evolved band-pass filter using an enhanced FPTA model; (B) – Frequency response (Axis X in Hz).

The new features can be observed from the schematic above: output and decoupling capacitances were added; and multiple paths from the input signal to the main circuit were allowed. It may be noted that the Genetic Algorithm did not start from scratch in this application because both capacitors' positions and values were known a priori from another evolved design [14]. However, the final frequency response is well centered within the AM band, providing a gain of around 15 dB (typical of human made design for this circuit). In this experiment, a successful GA execution required the sampling of around 10^4 individuals.

6 Conclusions

This paper reviewed the basic features of the programmable chip under test at JPL, the FPTA. We described reconfigurable chips used in EHW. Contrasting with most of these devices, the FPTA provides the benefits of programmability at the transistor level. New experiments were described in this paper, showing that the FPTA architecture, though being fine grained, is flexible enough to map basic analog and digital circuits building blocks. We reported new evolutionary experiments, which

have given us support for developing an enhanced design of the FPTA, which will include new switches and programmable capacitors.

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